Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Canceled)

2. (Currently Amended) The device as claimed in claim ~~1~~ 18 wherein when operated in bit serial fashion, the device provides hardware minimization of a finite impulse response filter~~, an infinite impulse response filter or for other filters, and application related to combinational logic consisting of delay elements [T], multiplier elements [M], and FA and/or FS elements~~.

3. (Currently Amended) The device as claimed in claim ~~1~~ 18 wherein ~~block [D] uses an FS~~ one of the combinational logic blocks includes a full subtracter element ~~instead of an FA element~~ when a ~~filter transfer function~~ coefficient value of the filter transfer function is close to a power of two.

4. (Currently Amended) The device as claimed in claim ~~1~~ 18 wherein ~~block [D] minimizes the use of FS elements by using~~the architecture includes a common subtraction operator ~~and substituting FA elements instead~~that operates with the full adder elements to minimize the use of full subtracter elements.

5. (Currently Amended) The device as claimed in claim ~~1~~ 18 wherein a first one of the coefficient lines ~~CLin_0... Clin_n are not derived from~~ is directly connected to a common input line, the delay blocks are sequentially connected to the common input line, and the remaining coefficient lines are coupled respectively to respective outputs of the delay blocks ~~but are instead respectively delayed by 0...n unit delays prior to input into said architecture [A]~~.

6. (Canceled)

7. (Currently Amended) A serial bit, ~~serial~~ finite impulse response (FIR) filter device including:

a logic block ~~[A] adapted to receive~~that receives an (m+1)-bit input and ~~to produce~~ produces a transfer function output corresponding to ~~the~~ an m^{th} bit position, the logic block ~~[A]~~ including:

a combinational-sequential logic block ~~[D] adapted to receive~~that receives ~~a~~ filter transfer function coefficients ~~S1, S2, ...Sn or~~of a predetermined filter transfer function, the combinational-sequential logic block ~~and~~ including m+1 combinational logic blocks B0, B1, ...Bm; and

a sequential logic block ~~[C]~~ having m delay elements ~~T1, T2, ...Tm~~ for receiving respective outputs of the combinational logic blocks B0, B1, ...Bm-1 and for providing delayed outputs to respective inputs of the combinational logic blocks B1, B2, ...Bm, respectively;

wherein each combinational logic block ~~Bx, for x=0,1...m,~~ includes a plurality of serial subtractor or adder elements ~~[SA], up to a maximum of n, SAx_1, SAx_2...SAx_n,~~ for providing a coefficient multiplication function for each ~~block Bx~~the combinational logic block; ~~and~~

wherein the combinational logic block Bm outputs said transfer function output according to said filter transfer function, based on said (m+1)-bit input; and

wherein each sequential subtractor or adder element includes a carry-out pin fed to an input of one of the sequential subtractor or adder elements of a previous one of the combinational logic blocks, such that the same delay element is used for multiplication by a factor of two and also for a carry function.

8. (Currently Amended) A digital filter device comprising:

a coefficient circuit having *n* input bits corresponding to *n* filter coefficients;

a combinational circuit comprising a plurality of full adders with the interconnection of the plurality of full adders depending on values of the *n* coefficients to implement the addition terms of the filter transfer function; and

a sequential circuit comprising a predetermined number of unit delays with the predetermined number being dependent on a maximum value of the *n* coefficients, the inputs of the unit delays being coupled to output of selected ones of the full adders and the output of the unit delays being coupled to an input of ~~a~~ one of the full ~~adder~~ adders of the combinational circuit in ~~an adjacent~~following bit position from the corresponding unit delay, wherein each of the full adders includes a carry-out pin fed to an input of one of the full adders in a previous bit position, such that the same unit delay is used for multiplication by a factor of two and also for a carry function.

9. (Currently Amended) The filter device of claim 8 wherein the combinational circuit implements the addition terms of the filter transfer function using the following form:

(a0*S1+b0*S2+...+k)*Sn),

(a1*S1+b1*S2+...+k1*Sn),

...

(am*S1+bm*S2+...+km*Sn)],

where S1, S1, Sn are ~~filter coefficients~~the input bits and

a0, b0...k0, a1, b1...k1, am, bm, ...km ~~are (~~each has a value of +/-1 or 0~~)~~.

10. (Currently Amended) The filter device of claim 8 wherein the coefficient circuit receives *n* serial input bits.

11. (Currently Amended) The filter device of claim 8 wherein the combinational circuit and the sequential circuit are interconnected to implement a finite input response (FIR) filter.

12. (Currently Amended) The filter device of claim 8 wherein the combinational circuit and the sequential circuit are interconnected to implement an infinite input response (IIR) filter.

13. –17. (Canceled)

18. (New) A filter device, comprising:

a plurality of delay blocks;

a plurality of coefficient lines coupled respectively to the delay blocks;

a logic architecture that includes:

serial input bit lines S1, S2, ... Sn coupled to the plurality of coefficient lines, n representing a number of coefficients of a filter transfer function; and

m combinational logic blocks having full adder elements and providing addition terms of the filter transfer function [(a0*S1+b0*S2+...+k)*Sn), (A1*S1+b1*S2+...+k1*Sn)...(am*S1+bm*S2+...+km*Sn)], where a0, b0...k0, a1, b1...k1, am, bm, ...km are coefficients having values of +/-1 or 0; wherein the full adder elements have respective first inputs, second inputs, and third input, the first inputs of the full adder elements being connected to the serial input bit lines S1, S2... Sn and to each other depending on the coefficients a0...km; wherein each full adder element includes a carry-out pin coupled to the third input of one of the full adder elements of a previous one of the combinational logic blocks; wherein the combinational logic blocks include respective output lines b_1, b_2, ... b_m, and the output line b_m provides a final output of the architecture; and

a sequential logic cluster having a plural number of delay elements depending on a size of a maximum coefficient value of the filter transfer function, each delay element having an input coupled to a respective one of the output lines of the combinational logic blocks and an output coupled to the second input of one of the full adder elements of a respective combinational logic block corresponding to a next bit position such that the same delay element is used for multiplication by a factor of two and also for a carry structure in a one bit serial adder

function, wherein the delay elements are respectively positioned adjacent to respective end positions of respective combinational logic blocks.